

Approved	0.2.16
BY	C. S. S. / S. H. S.
FOR	FOR

FIG.1

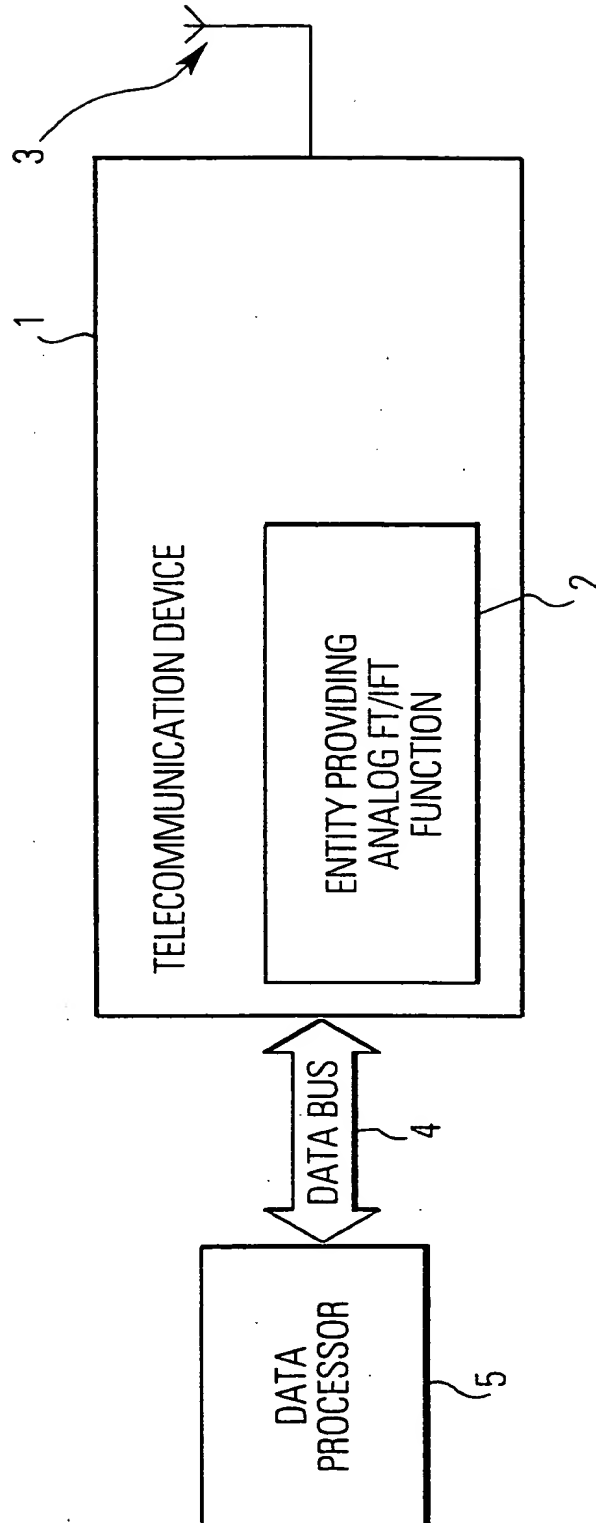


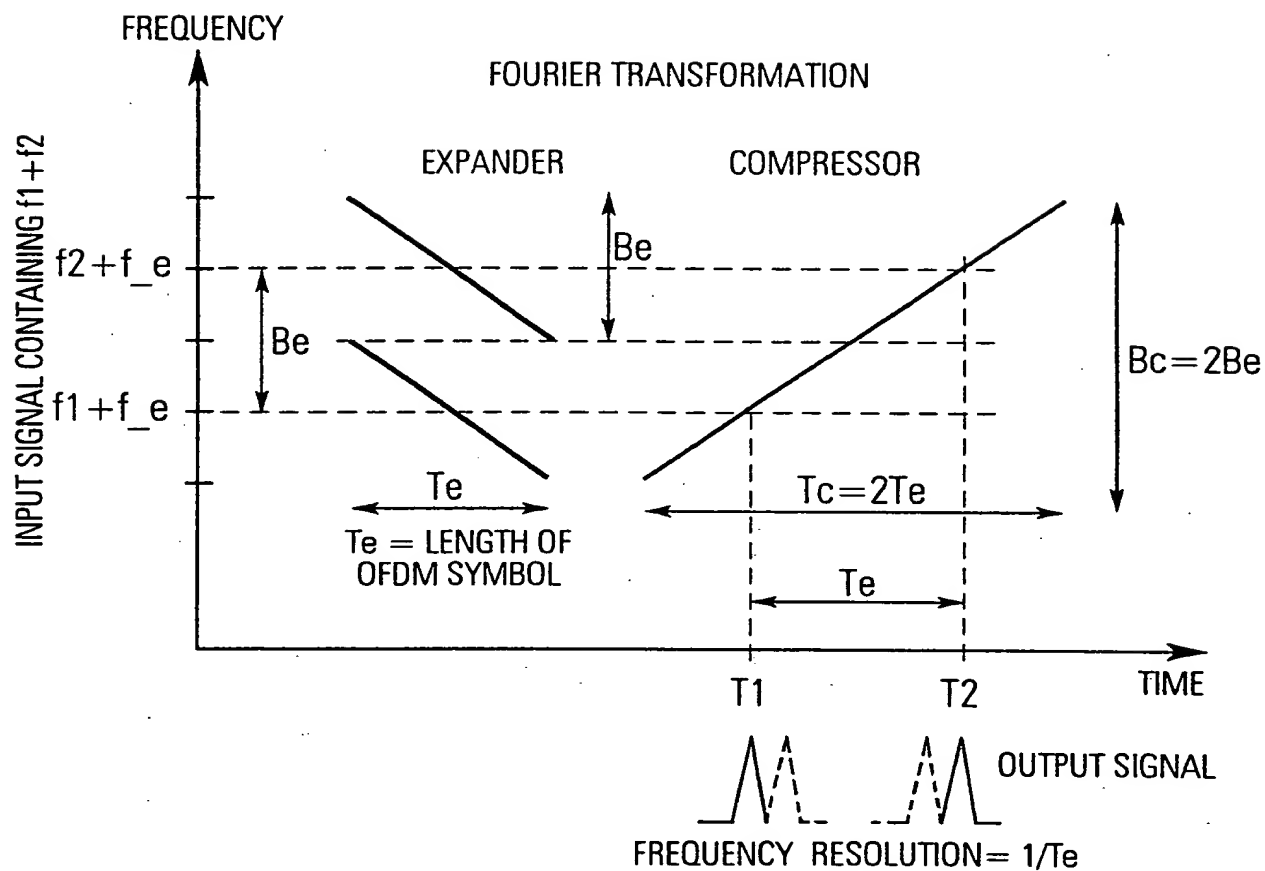
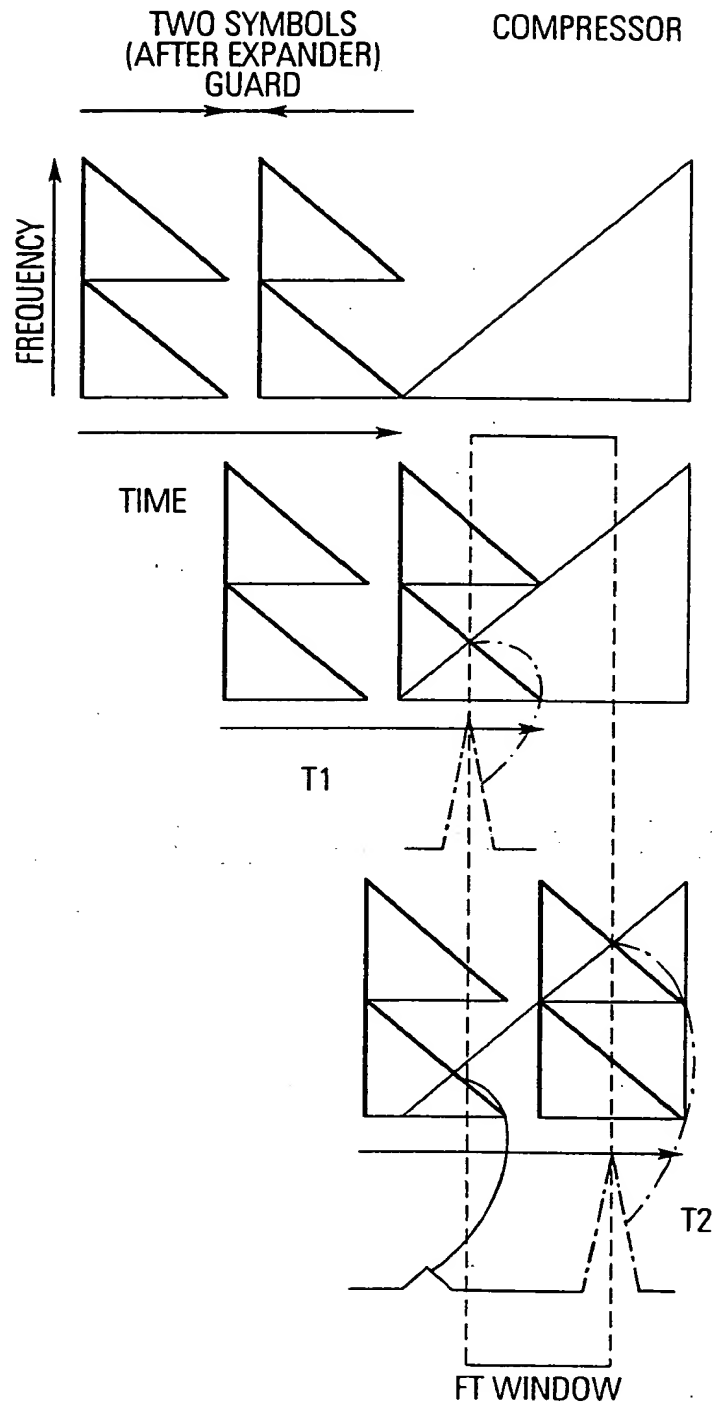
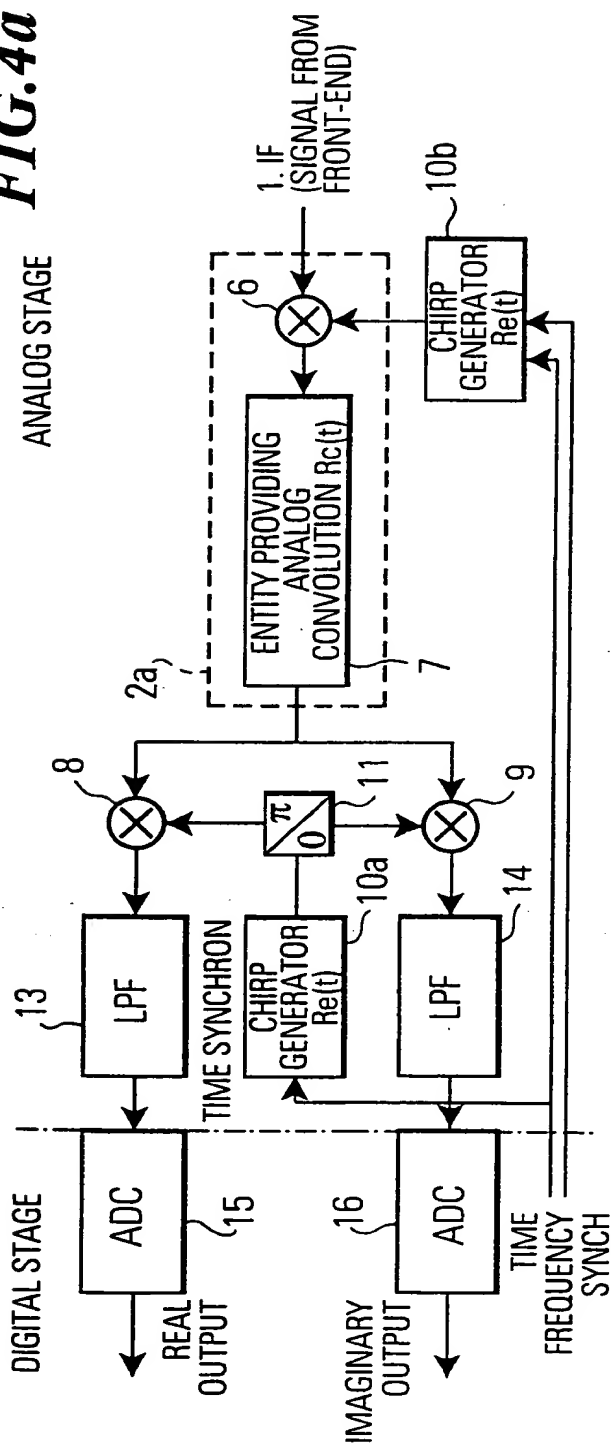
FIG.2

FIG.3



ANALOG STAGE



ANALOG STAGE

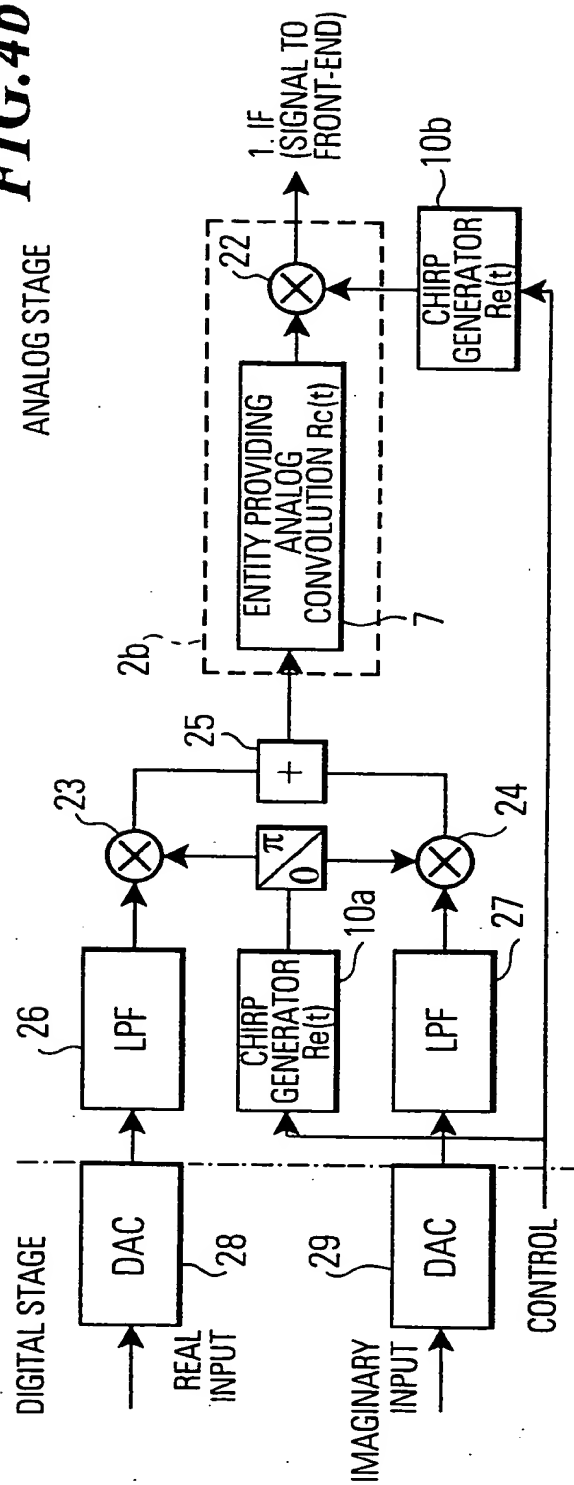


FIG. 5a

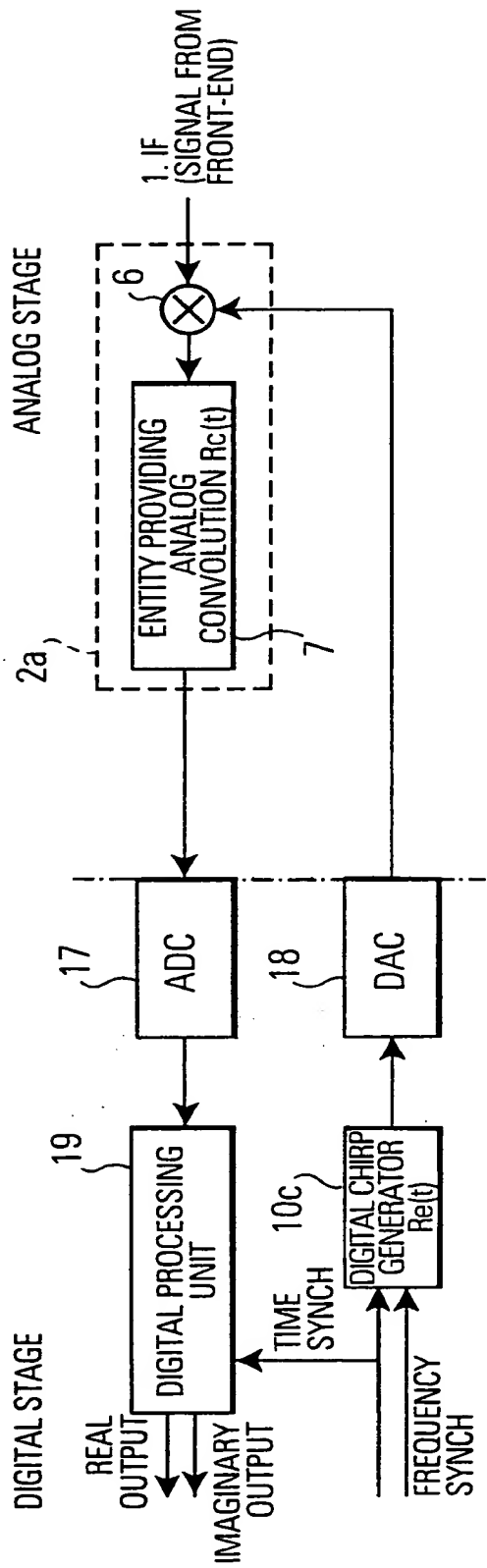
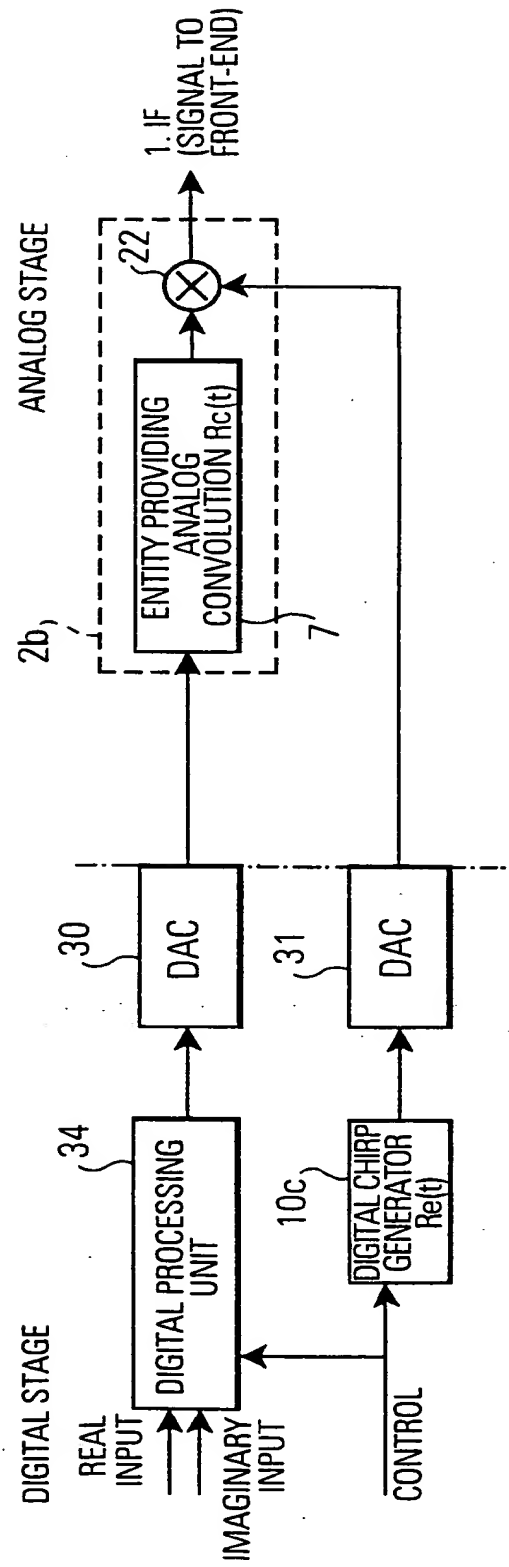


FIG. 5b



The diagram illustrates a digital baseband processor architecture, divided into a **DIGITAL STAGE** and an **ANALOG STAGE**.

DIGITAL STAGE:

- CORDIC (20):** Receives **TIME SYNCH** and **FREQUENCY SYNCH** signals. It has bidirectional data flow with the **IQ GENERATOR (21)**.
- IQ GENERATOR (21):** Outputs **REAL OUTPUT** and **IMAGINARY OUTPUT**.
- DAC (18):** Receives digital data from the **DIGITAL CHIRP GENERATOR (10c)** and outputs an analog signal to the **ADC (17)**.
- DIGITAL CHIRP GENERATOR (10c):** Receives **FREQUENCY SYNCH** and outputs digital data to the **DAC (18)**.

ANALOG STAGE:

- ADC (17):** Receives the analog signal from the **DAC (18)** and outputs digital data to the **ENTITY PROVIDING ANALOG CONVOLUTION $R_c(t)$ (7)**.
- ENTITY PROVIDING ANALOG CONVOLUTION $R_c(t)$ (7):** A functional block that receives digital data from the **ADC (17)** and outputs an analog signal to the multiplier **6**.
- Multiplier (6):** Receives the analog signal from the **ENTITY PROVIDING ANALOG CONVOLUTION $R_c(t)$ (7)** and the **1. IF (SIGNAL FROM FRONT-END)** signal. Its output is the final analog signal.

The diagram illustrates a digital-to-analog converter system, divided into a DIGITAL STAGE and an ANALOG STAGE.

DIGITAL STAGE:

- REAL INPUT** and **IMAGINARY INPUT** feed into a **CORDIC** block (20).
- A **DIGITAL CHIRP GENERATOR** (10c) receives **FREQUENCY SYNCH** input and provides a signal to the **CORDIC** block (20) and a **DAC** (31).
- The **CORDIC** block (20) outputs to a **DAC** (30).

ANALOG STAGE:

- The output of **DAC** (30) and a signal from the **DIGITAL CHIRP GENERATOR** (10c) feed into an **ENTITY PROVIDING ANALOG CONVOLUTION** block (7).
- The output of block (7) is multiplied by a signal (22) to produce the final **1.IF (SIGNAL TO FRONT-END)** output.

FIG. 7a

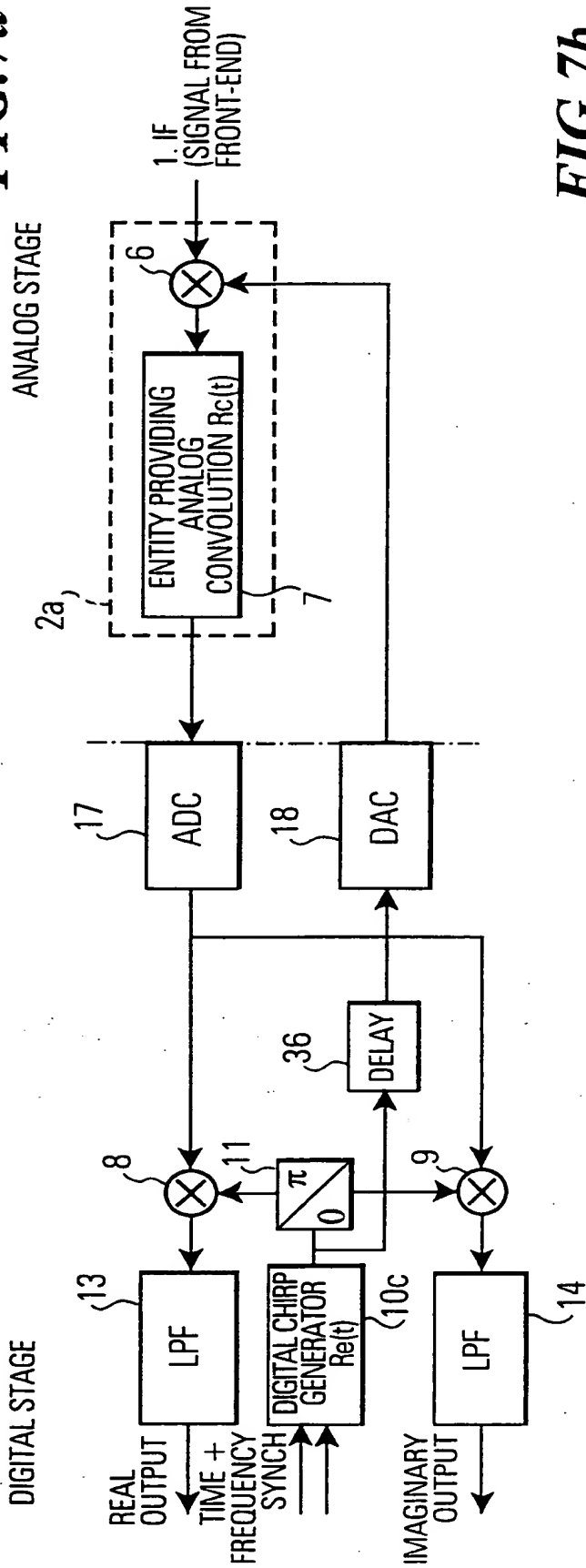


FIG. 7b

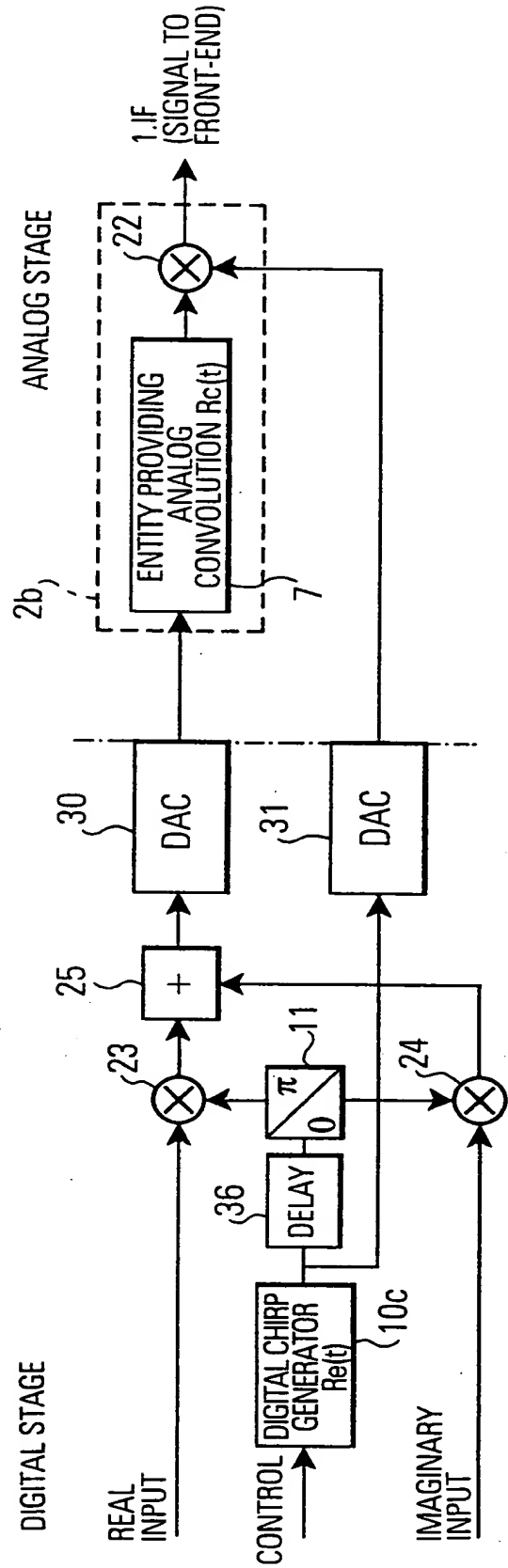
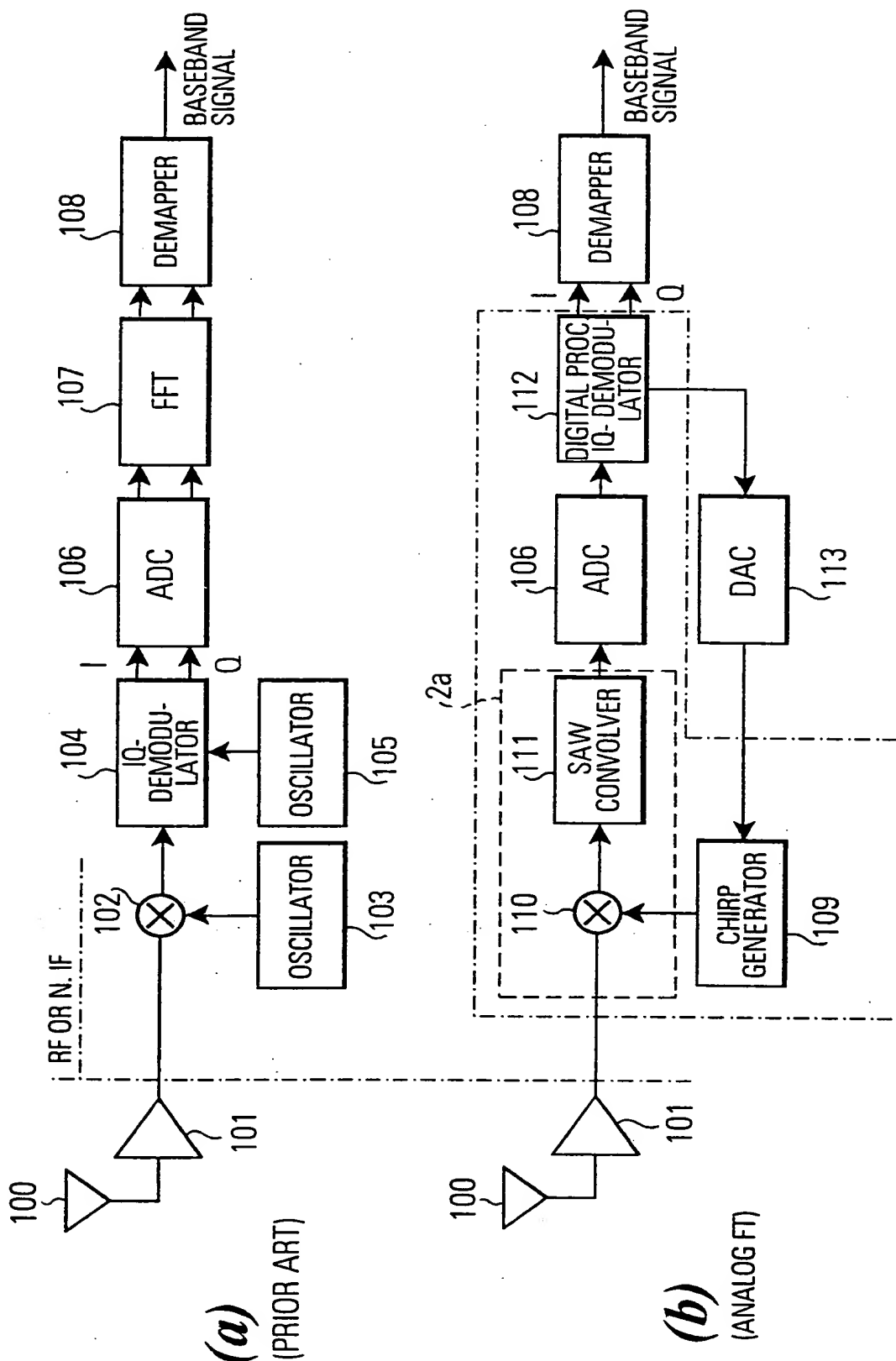


FIG.8 OFDM RECEIVER



DISTRIBUTED FFT: FFT IS PERFORMED OVER SEVERAL DEVICE ENTITIES

Fig. 9

